REMARKS

Preliminarily, Applicants appreciate the Examiner's courtesy in granting the interview of October 8, 2002. Therein, the Examiner reiterated that the capacitor formed as a part of the multilayer substrate in Zavrel necessarily occupies space within the substrate, and that such space is within the scope of the claimed "capacitor accommodation cavity".

Review and reconsideration on the merits are requested.

Claims 1-13 and 16-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,218,729 to Zavrel, Jr. et al. The grounds for rejection remain the same as set forth in the previous Office Action.

As pointed out in the remarks portion of the Amendment Under 37 C.F.R. § 1.111 filed July 11, 2002, Applicants respectfully disagree because capacitor plates 860 and 862 of Zavrel et al are embedded in the laminated substrate 822 and a capacitor accommodation cavity is not disclosed. Rather, the substrate of the Zavrel et al has a laminated structure of interconnects, where passive devices such as capacitor 804 are designed into the metal interconnect layers. There is no hollow area within the substrate for accommodating a capacitor or other components.

However, to advance prosecution of this application, claims 1, 2 and 4 have been amended to recite that the printed wiring substrate comprises a capacitor accommodation cavity selected from a closed-bottom cavity and a through hole cavity extending in the thickness direction of the printed wiring substrate and a capacitor disposed in said cavity. Support is found, for example, at page 16, lines 8-12 of the specification. In this manner, the capacitor terminals and the substrate terminals are densely located on and around the capacitor. Therefore, the planar size of the IC chip to be connected to the terminals can be made as small as possible,

thereby providing an inexpensive capacitor-built-in-type printed wiring substrate on which the IC chip is mounted (page 15, line 16-page 16, line 7 of the specification). Even assuming that Zavrel inherently discloses a hollow area within the substrate for accommodating an embedded capacitor, Zavrel does not disclose (i) a capacitor accommodation cavity selected from a closed-bottom cavity and a through-hole cavity, and (ii) a capacitor disposed in said cavity as required by the amended claims. The amended claim language differs from the original claim language in that the accommodation cavity is specifically defined, and further requires a capacitor disposed in said cavity. Zavrel selectively etches metal interconnect layers, resulting in an embedded capacitor different from a capacitor disposed in a capacitor accommodation cavity.

It is respectfully submitted that the claims as amended patentably distinguish over Zavrel, and withdrawal of the foregoing rejection under 35 U.S.C. § 102(e) is respectfully requested.

Withdrawal of all rejections and allowance of claims 1-13 and 16-18 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Four times amended) A printed wiring substrate having a planar surface and a built-in capacitor on which an IC chip is mounted, said printed wiring substrate comprising a capacitor accommodation cavity [for accommodating the capacitor] selected from the group consisting of a closed-bottom cavity and a through hole cavity extending in the thickness direction of the printed wiring substrate and a capacitor disposed in said cavity, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively flip-chip-bonded directly to a plurality of connection-to-capacitor terminals of the IC chip; and

the plurality of substrate terminals of the printed wiring substrate are respectively flip-chip-bonded to a plurality of connection-to-substrate terminals of the IC chip.

2. (Four times amended) A printed wiring substrate having a planar surface and a built-in capacitor on which an IC-chip-carrying printed wiring substrate is mounted, said printed wiring substrate comprising a capacitor accommodation cavity [for accommodating the capacitor] selected from the group consisting of a closed-bottom cavity and a through hole cavity extending in the thickness direction of the printed wiring substrate and a capacitor disposed in said cavity, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip-carrying printed wiring circuit comprises a plurality of connection-to capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively bonded in a connection-face-to-connection-face manner directly to a plurality of connection-to-capacitor terminals of the IC-chip-carrying printed wiring substrate; and

the plurality of substrate terminals of the printed wiring substrate are respectively bonded in a connection-face-to-connection-face manner to a plurality of connection-to-substrate terminals of the IC-chip-carrying printed wiring substrate.

4. (Three times amended) A printed wiring substrate having a planar surface and a built-in capacitor for mounting an IC chip or IC-chip-carrying printed wiring substrate having a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals, said printed wiring substrate comprising a capacitor accommodation cavity [for accommodating the capacitor] selected from the group consisting of a closed-bottom cavity and a through hole cavity extending in the thickness direction of the printed wiring substrate and a capacitor disposed in said cavity, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner to a plurality of connection-to-capacitor terminals of the IC chip or IC-chip-carrying printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode group; and

the printed wiring substrate comprises a plurality of substrate terminals capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner directly to a plurality of connection-to-substrate terminals of the IC chip or IC-chip-carrying printed wiring substrate.